Input/output buffer with high voltage endurance and good electrostatic discharge endurance

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Zusammenfassung von **TW449968B**

The present invention provides an input/output buffer with high voltage endurance. The I/O buffer of the present invention comprises a pad, a driving PMOS, a buffer NMOS and a driving NMOS. The pad is coupled to a protection circuit between high power and low power lines. The driving PMOS has a floating base, a source coupled to the high power line and a drain coupled to the pad. The buffer NMOS has a gate coupled to the high power line, and a drain coupled to the pad. The driving NMOS has a drain coupled to the source of the buffer NMOS, and a source coupled to the low power line. When a positive ESD event relative to the low power line occurs at the pad, the protection circuit between the power lines will be triggered to reduce the voltage of the high power line, and turn off the buffer NMOS through the high power line. Thereby, the ESD current won't flow through the surface channel of the driving NMOS connected in series, which can protect the driving NMOS from the damage of ESD stress.